Abstracts

When are transmission-line effects important for on-chip interconnections?

A. Deutsch, G.V. Kopcsay, P.J. Restle, H.H. Smith, G. Katopis, W.D. Becker, P.W. Coteus, C.W. Surovic, B.J. Rubin, R.P. Dunne, T. Gallo, K.A. Jenkins, L.M. Terman, R.H. Dennard, G.A. Sai-Halasz, B.L. Krauter and D.R. Knebel. "When are transmission-line effects important for on-chip interconnections?." 1997 Transactions on Microwave Theory and Techniques 45.10 (Oct. 1997, Part II [T-MTT] (Special Issue on Interconnects and Packaging)): 1836-1846.

Short, medium, and long on-chip interconnections having linewidths of 0.45-52 /spl mu/m are analyzed in a five-metal-layer structure. We study capacitive coupling for short lines, inductive coupling for medium-length lines, inductance and resistance of the current return path in the power buses, and line resistive losses for the global wiring. Design guidelines and technology changes are proposed to achieve minimum delay and contain crosstalk for local and global wiring. Conditional expressions are given to determine when transmission-line effects are important for accurate delay and crosstalk prediction.

❑ Return to main document.